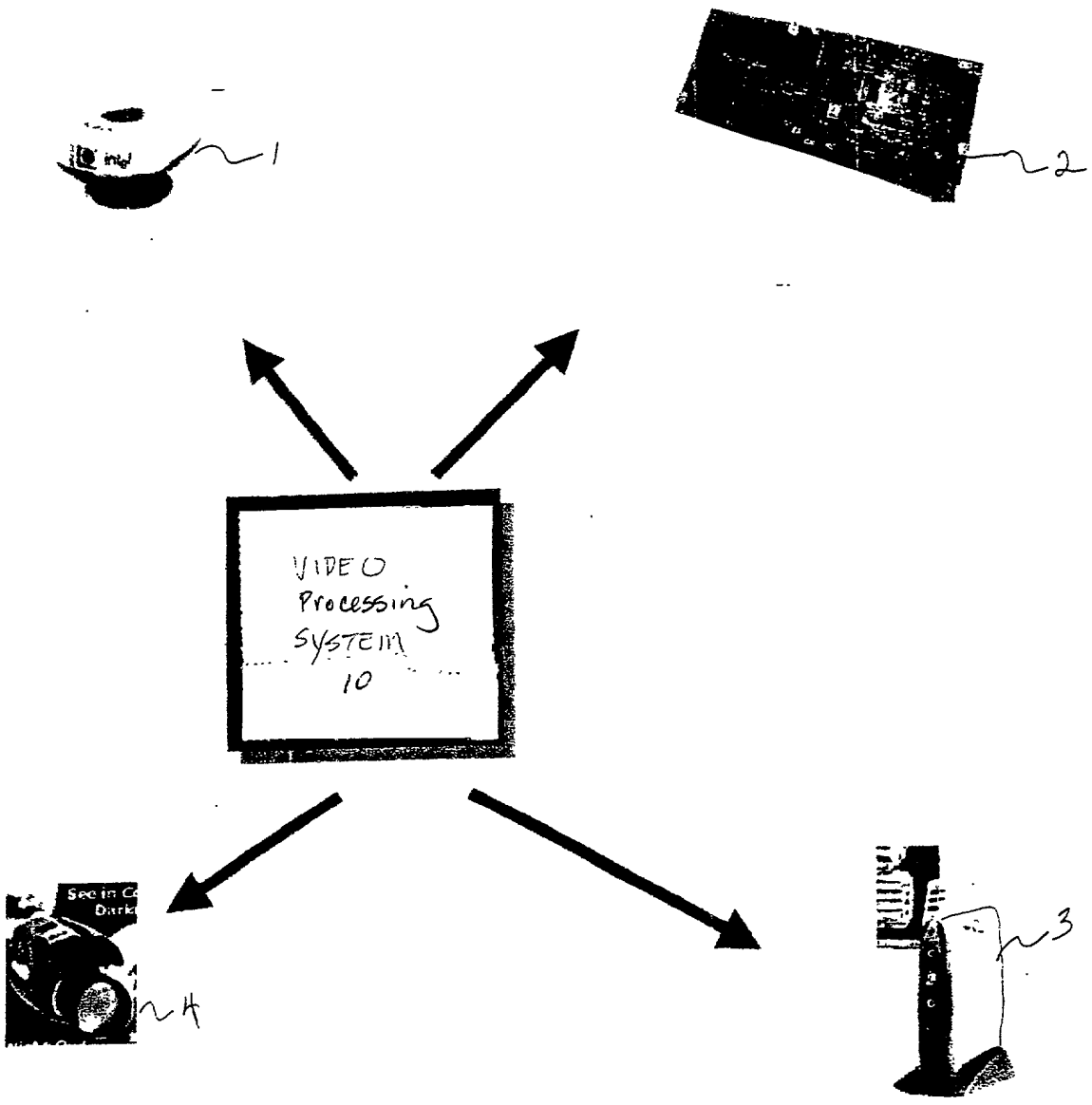


FIG. 1A

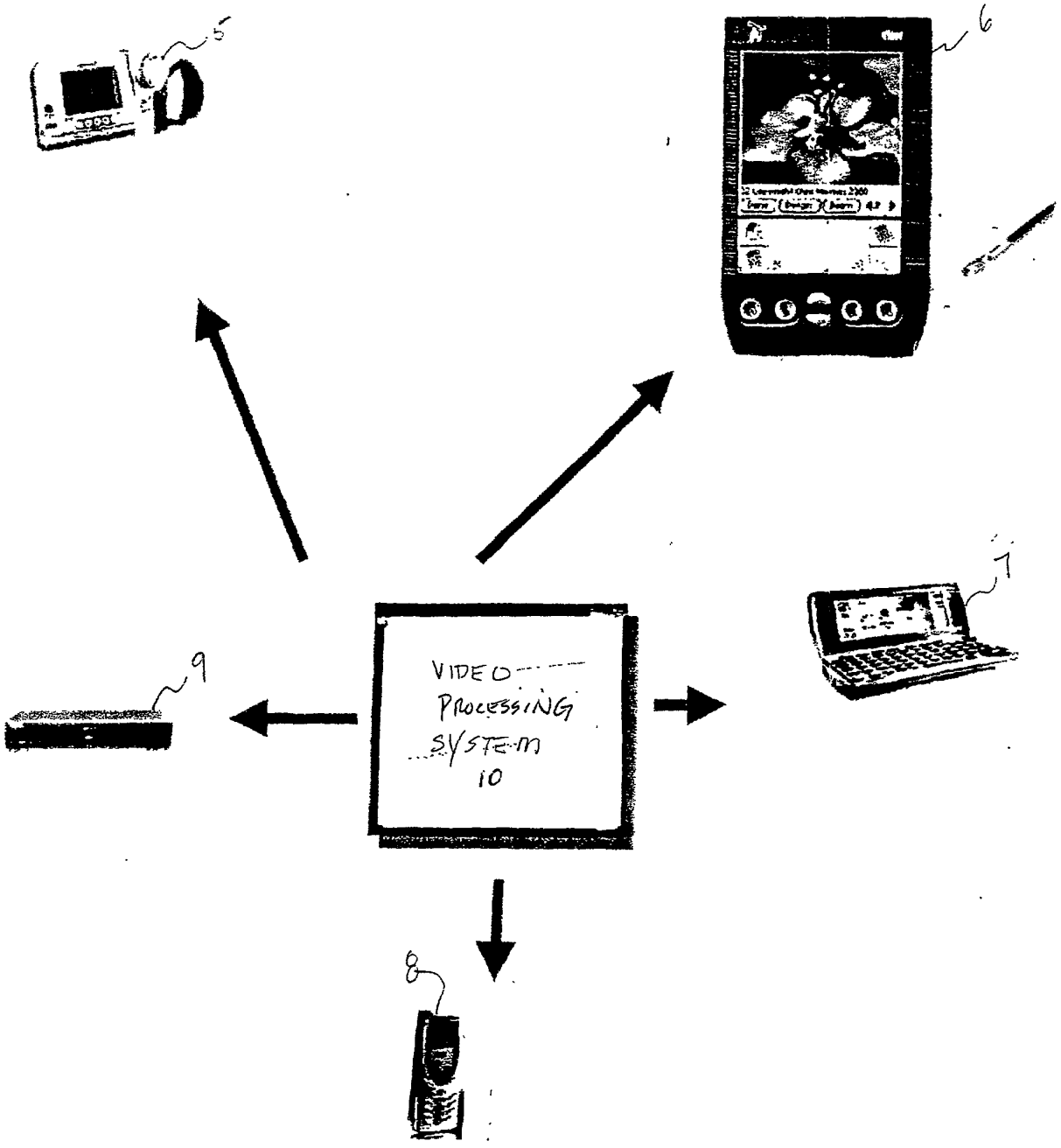


FIG. 1B

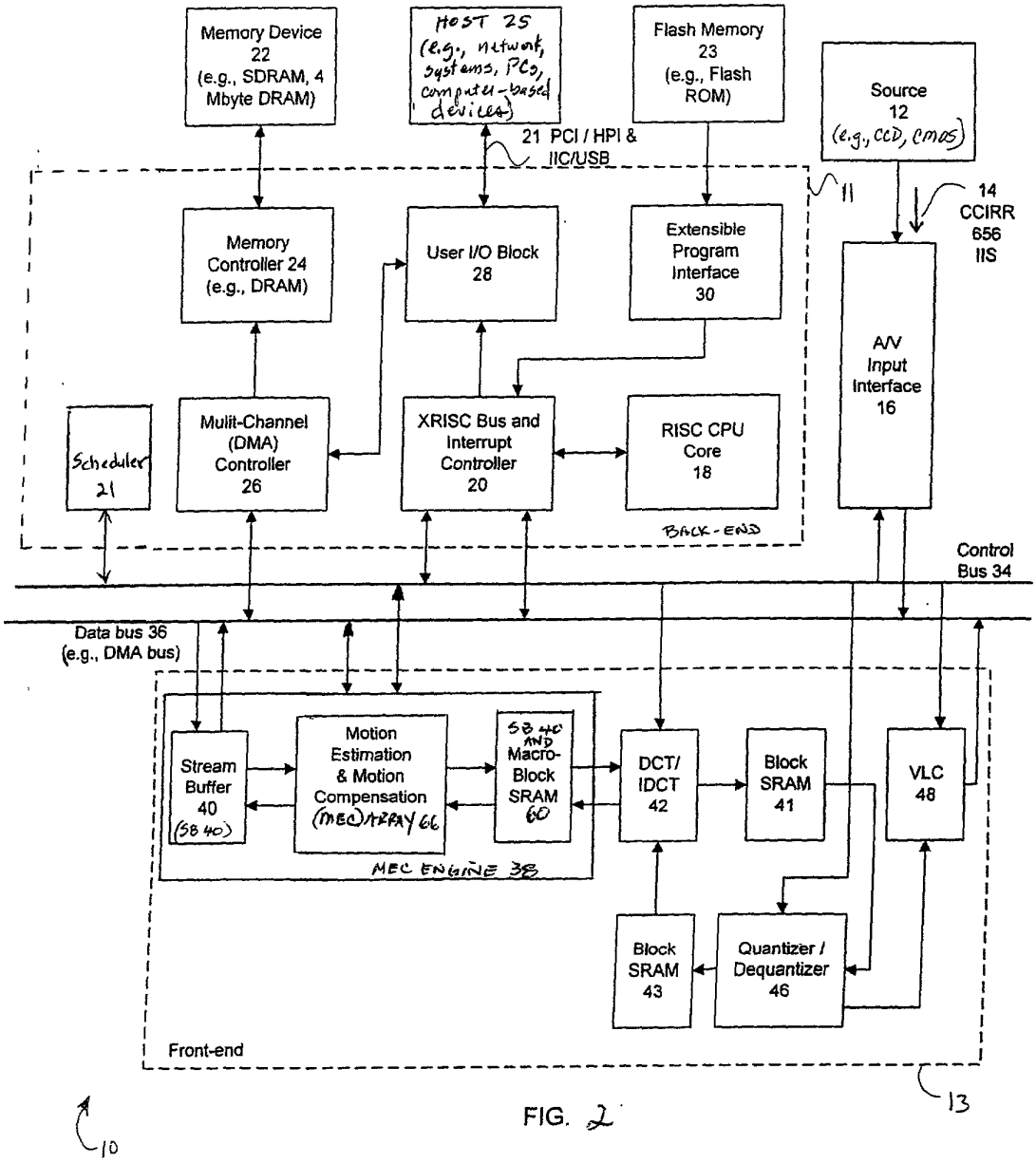
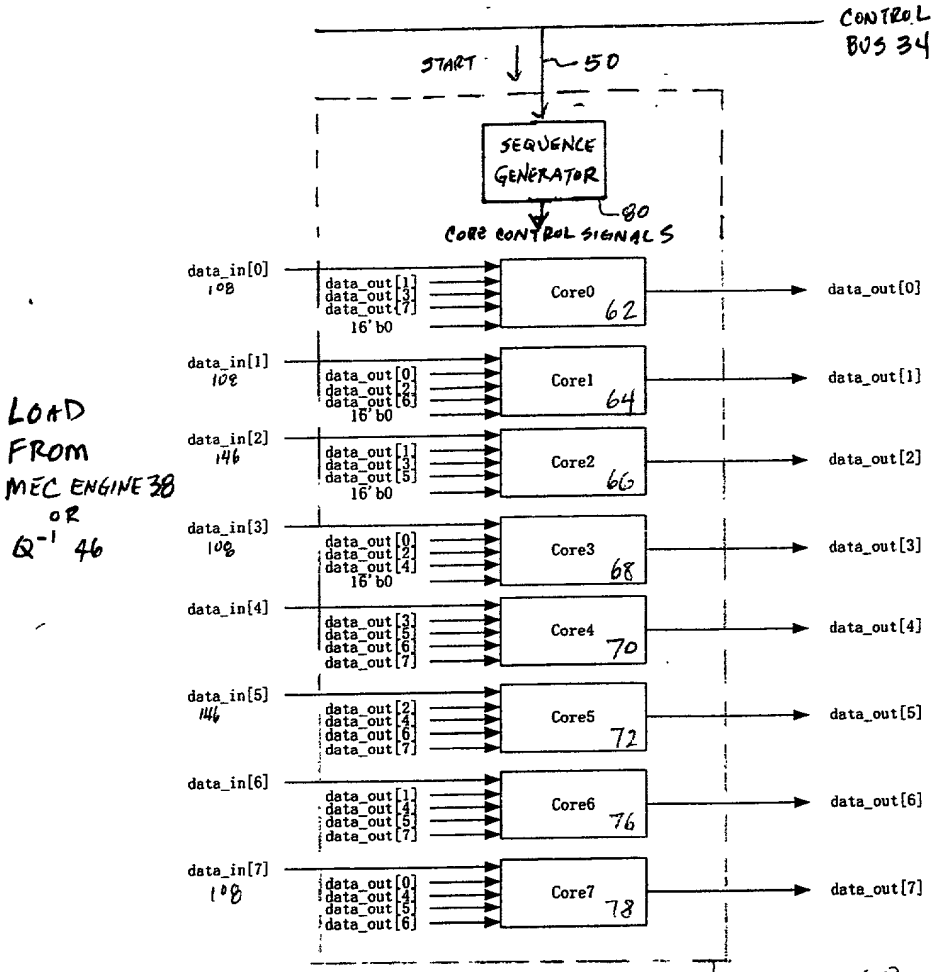

Memory Device 22 (e.g., SDRAM, 4 Mbyte DRAM)
HOST 25 (e.g., network, systems, PCs, computer-based devices)
Flash Memory 23 (e.g., Flash ROM)
Source 12 (e.g., CCD, CMOS)
21 PCI / HPI & IIC/USB
11
14 CCIRR 656 IIS
Memory Controller 24 (e.g., DRAM)
User I/O Block 28
Extensible Program Interface 30
A/V Input Interface 16
Scheduler 21
Mulit-Channel (DMA) Controller 26
XRISC Bus and Interrupt Controller 20
RISC CPU Core 18
BACK-END
Control Bus 34
Data bus 36 (e.g., DMA bus)
Stream Buffer 40 (SB 40)
Motion Estimation & Motion Compensation (MEC) ARRAY 66
SB 40 AND Macro-Block SRAM 60
DCT/ IDCT 42
Block SRAM 41
VLC 48
MEC ENGINE 38
Block SRAM 43
Quantizer / Dequantizer 46
Front-end
13
10

FIG. 2



LOAD FROM MEC ENGINE 38 OR Q^{-1} 46

WRITE TO Q 46 OR TO DECOMPENSATION FOR DCT^{-1}

FIG. 3

Datapath of core0,core1,core3,core7

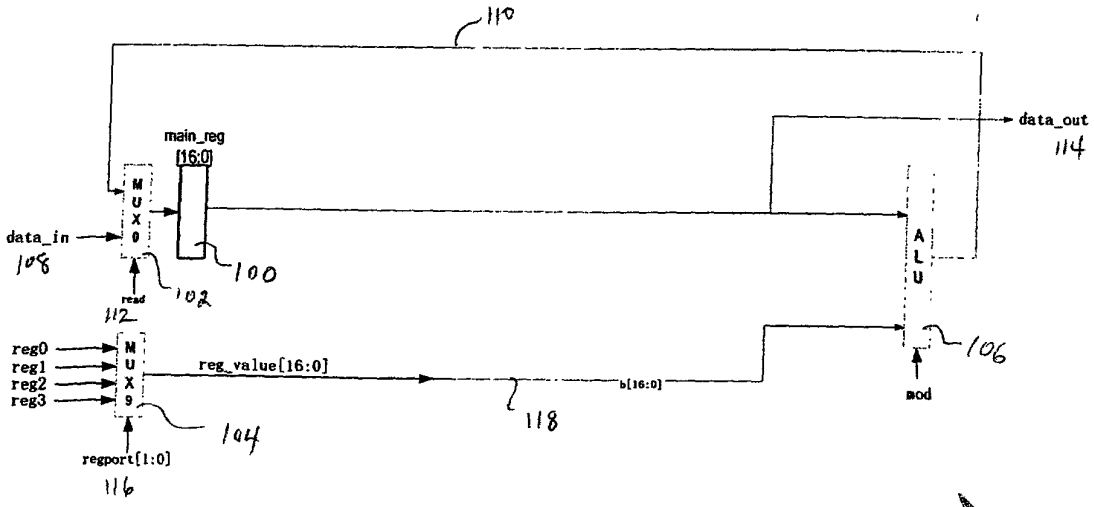


FIG. 4

62/64/68/78

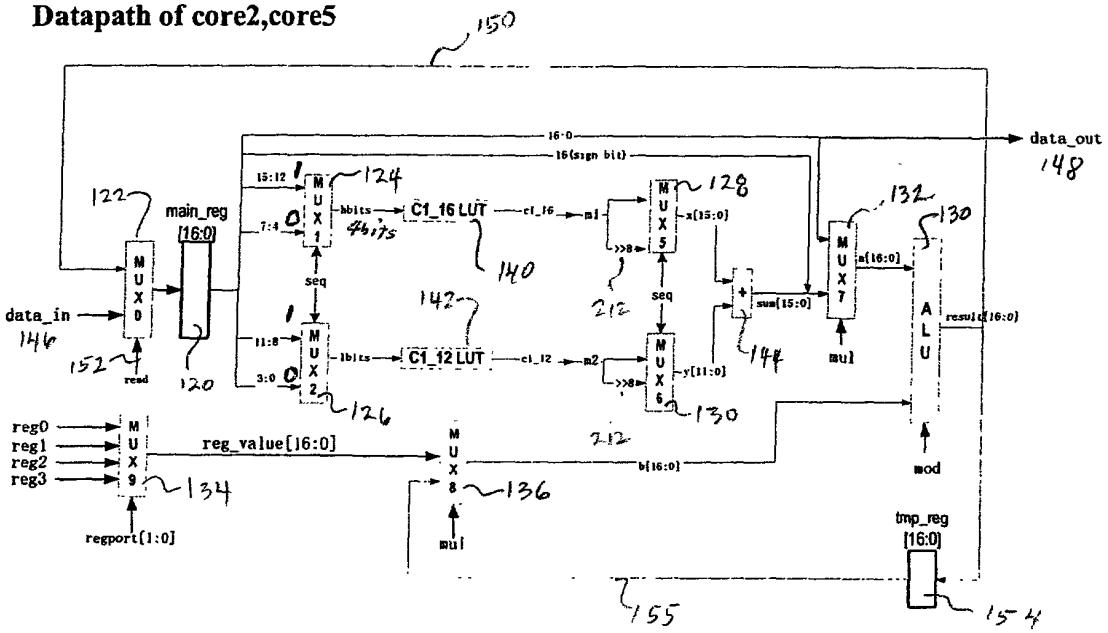

Datapath of core2,core5
150
data_out
148
16:0
16(sign bit)
122
main_reg
[16:0]
MUX0
data_in
146
152
read
120
MUX1
15:12
7:4
1
0
124
4bits
C1_16 LUT
140
c1_16
m1
MUX5
128
x[15:0]
>>8
212
seq
142
MUX2
11:8
3:0
1bits
C1_12 LUT
c1_12
m2
MUX6
130
y[11:0]
126
MUX7
132
130
a[16:0]
sum[15:0]
144
mul
ALU
result[16:0]
mod
reg0
reg1
reg2
reg3
MUX9
134
regport[1:0]
reg_value[16:0]
MUX8
136
mul
b[16:0]
tmp_reg
[16:0]
154
155

FIG. 5

Datapath of core6

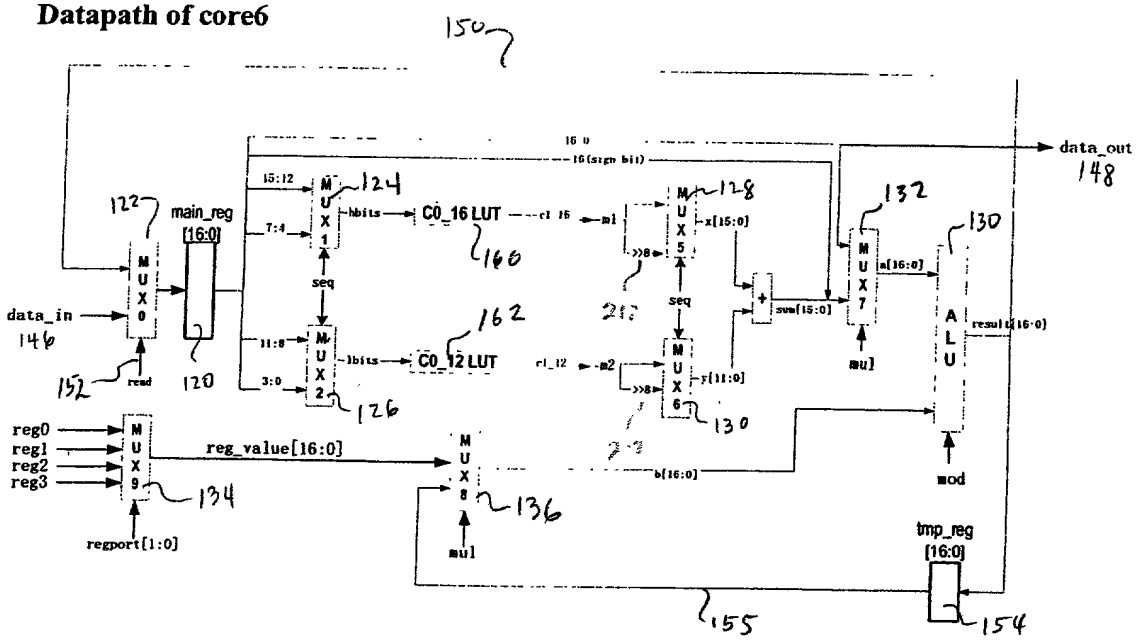


FIG. 6

76

Datapath of core4

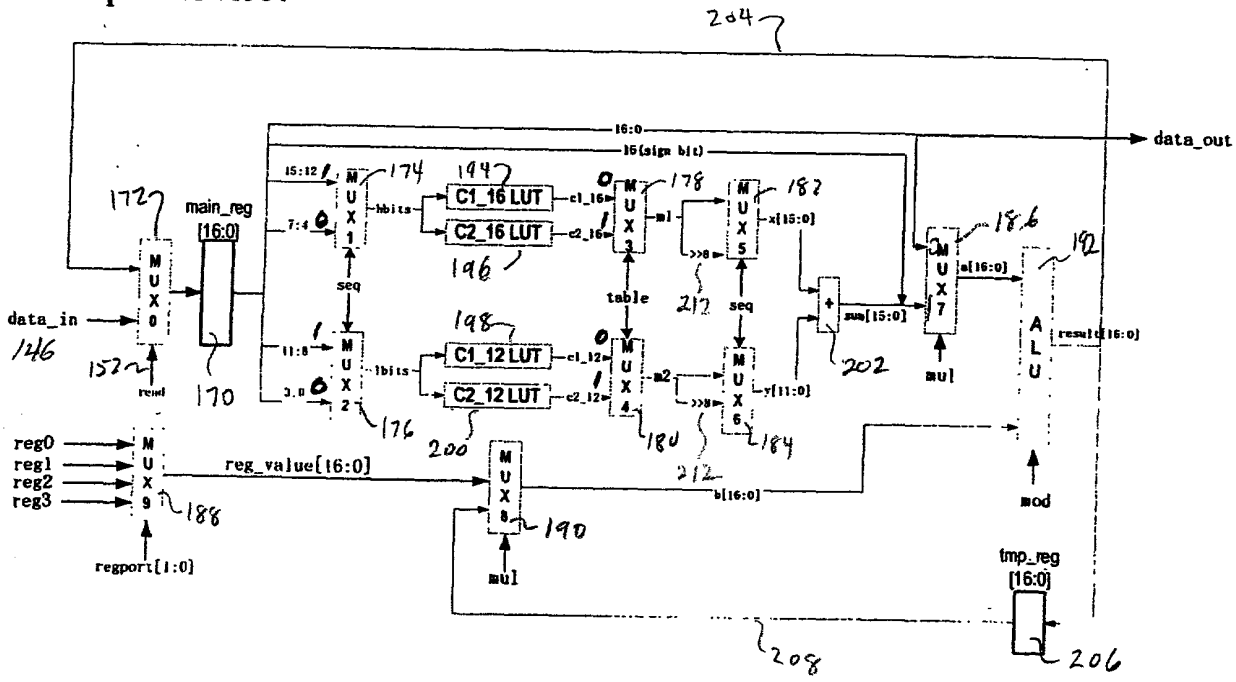


FIG. 7

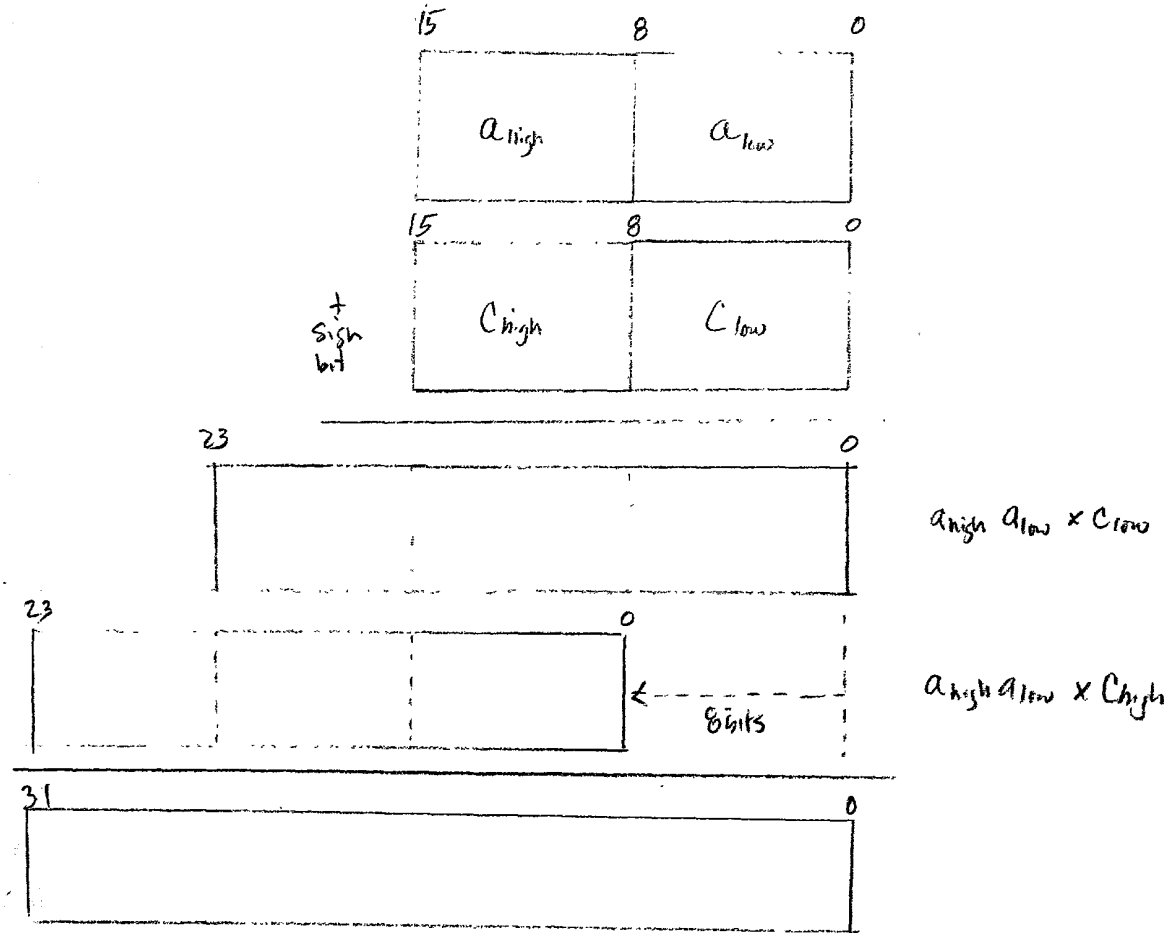

15
8
0
a_{high}
a_{low}
15
8
0
+
sign bit
C_{high}
C_{low}
23
0
a_{high} a_{low} × C_{low}
23
0
8bits
a_{high} a_{low} × C_{high}
31
0

FIG. 8A

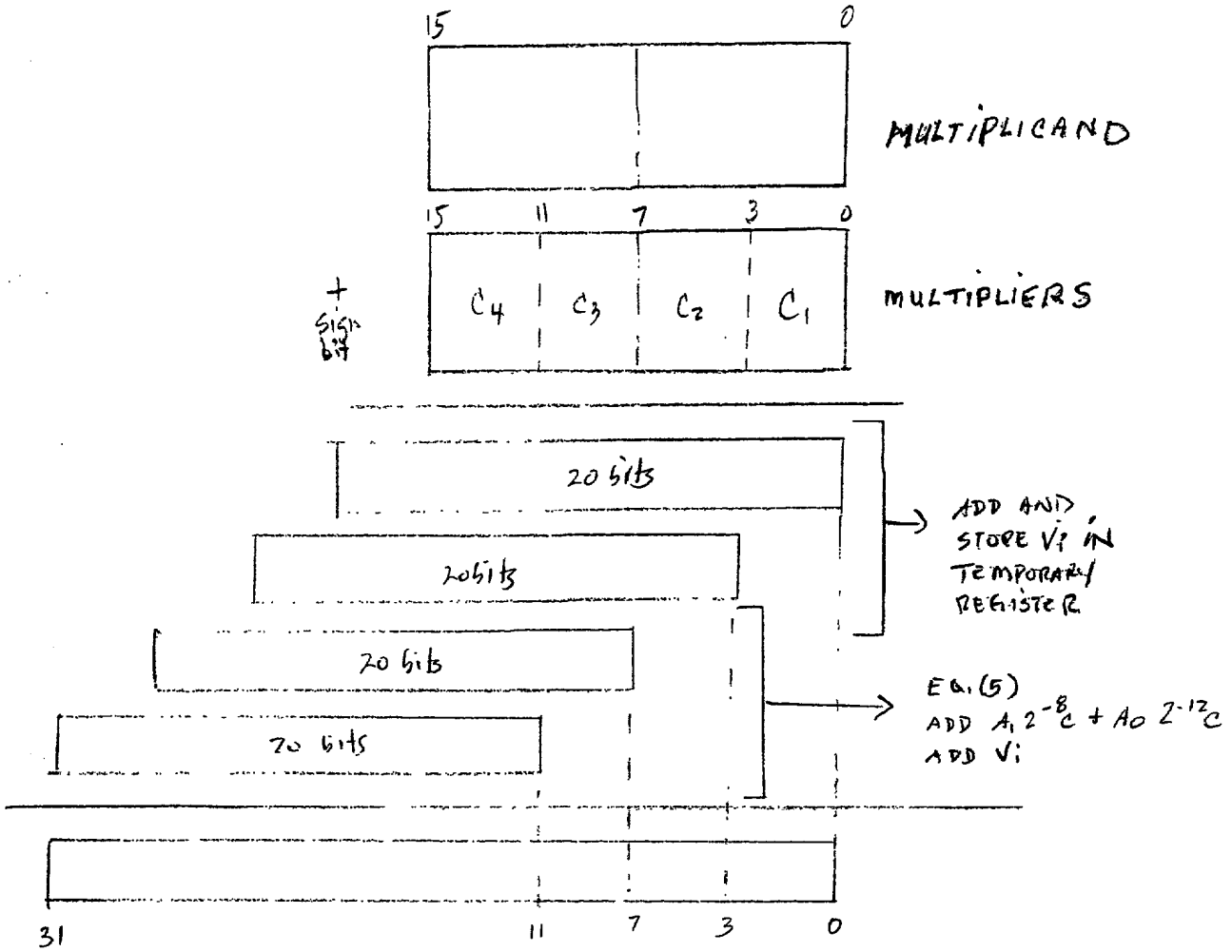

15
0
MULTIPLICAND
15
11
7
3
0
+ sign bit
C4
C3
C2
C1
MULTIPLIERS
20 bits
20 bits
20 bits
20 bits
ADD AND STORE Vi IN TEMPORARY REGISTER
EQ. (5)
ADD A1 2-8C + A0 2-12C
ADD Vi
31
11
7
3
0

FIG. 8B

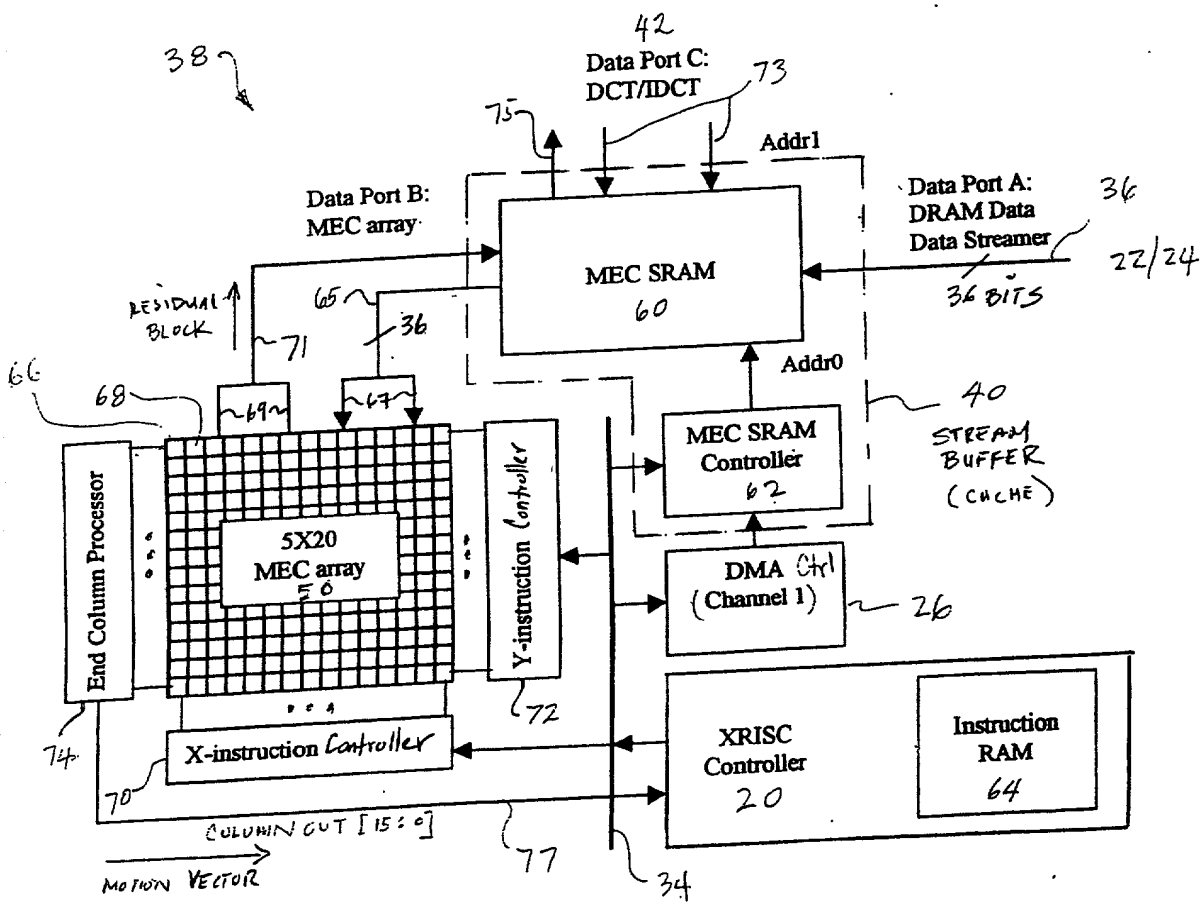

38
42
Data Port C:
DCT/IDCT
73
75
Addr1
Data Port B:
MEC array
Data Port A:
DRAM Data
Data Streamer
36
22/24
36 BITS
MEC SRAM
60
RESIDUAL BLOCK
65
36
71
Addr0
66
68
69
67
40
STREAM BUFFER (CACHE)
MEC SRAM Controller
62
End Column Processor
5X20
MEC array
50
Y-instruction Controller
DMA Ctrl
(Channel 1)
26
72
74
X-instruction Controller
70
XRISC
Controller
20
Instruction
RAM
64
COLUMN OUT [15:0]
77
34
MOTION VECTOR

FIG. 9

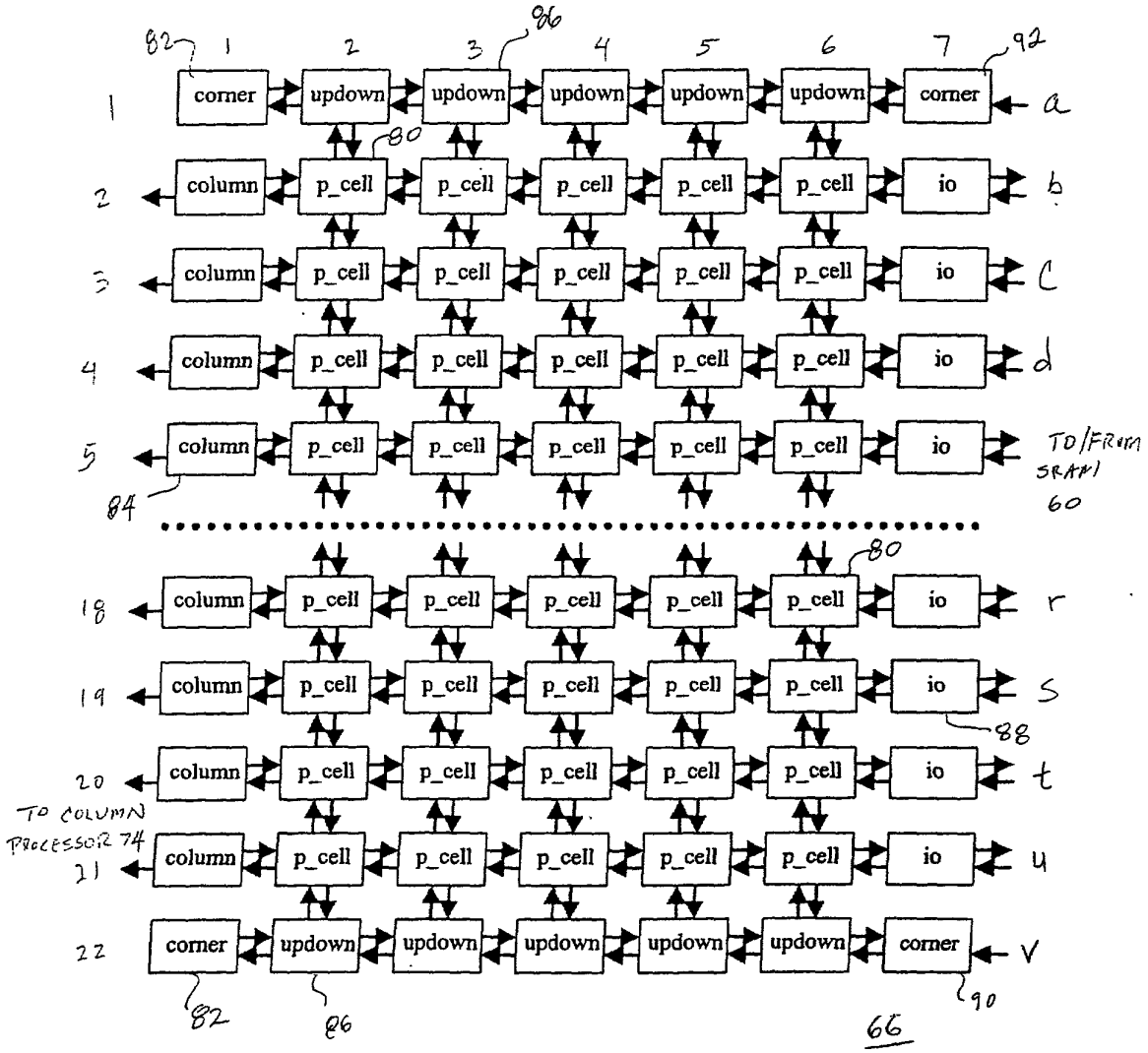

82
1
2
3
86
4
5
6
7
92
corner
updown
corner
a
80
column
p_cell
io
b
c
d
TO/FROM SRAM 60
84
r
s
88
t
u
v
TO COLUMN PROCESSOR 74
90
66

FIG. 10

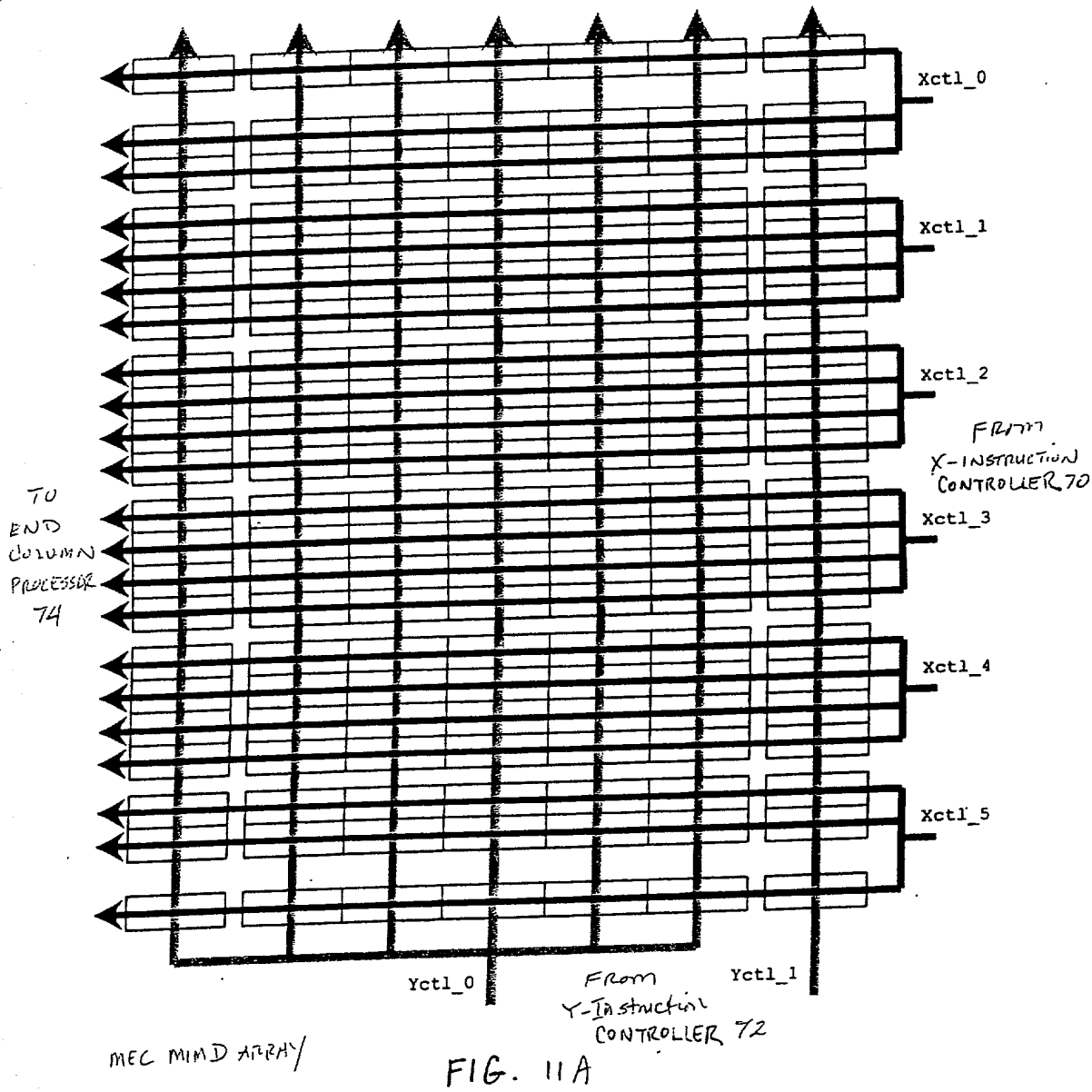

Xctl_0
Xctl_1
Xctl_2
FROM X-INSTRUCTION CONTROLLER 70
Xctl_3
Xctl_4
Xctl_5
TO END COLUMN PROCESSOR 74
Yctl_0
FROM Y-INSTRUCTION CONTROLLER 72
Yctl_1
MEC MIMD ARRAY

FIG. 11A

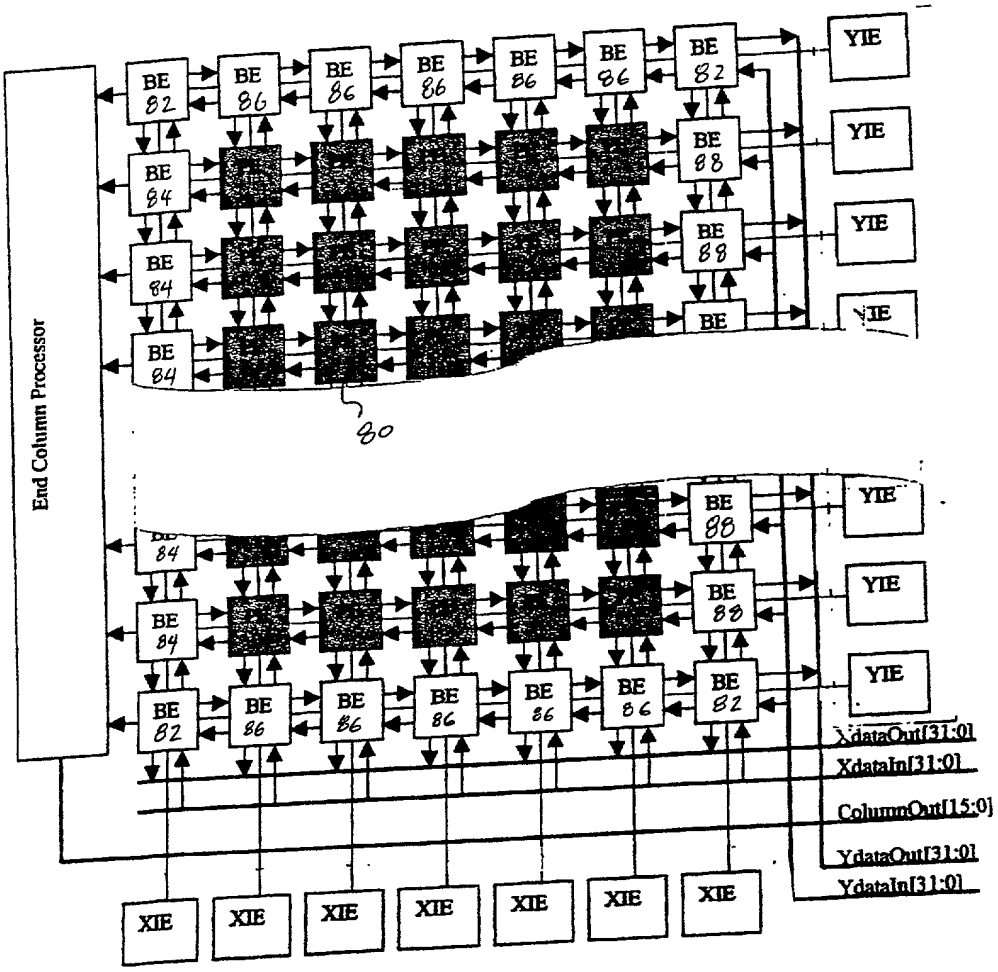

End Column Processor
BE 82
BE 86
BE 84
BE 88
YIE
XIE
80
XdataOut[31:0]
XdataIn[31:0]
ColumnOut[15:0]
YdataOut[31:0]
YdataIn[31:0]
Processor Element = p-cell 80
Boundary Element (82, 84, 86, 88)
X- Instruction Element 94
Y- Instruction Element 96
MEC SIMD array

FIG. 11B